CLAIMS

What is claimed is:

1. Counter arrangement comprising a plurality of counter registers and at least the same number of checksum registers being controlled by control means, whereby the counter control means change the content of only one of the counter registers for each change in the counting sequence and comprise means to update the checksum registers, whereby the content of each checksum registers is defined by an associated function which allows recovery of the content of each counter register and a function performed on the content of all checksum registers results in a constant value.

2. Counter arrangement according to claim 1, wherein respective sets of two counter registers from the plurality of counter registers are coupled with an associated checksum register through a functional unit.

3. Counter arrangement according to claim 2, wherein the functional unit performs a logical function.

4. Counter arrangement according to claim 2, wherein the functional unit performs an arithmetic function.

5. Counter arrangement according to claim 2, wherein the functional unit is an EXCLUSIVE OR gate.

6. Counter arrangement according to claim 1, wherein the control unit comprises an incrementer/decrementer unit selectively coupled with one of the counter registers.

7. Counter arrangement comprising:

- a control unit;

- first, second, and third registers coupled with said control unit;

- fourth, fifth, and sixth registers coupled with said control unit;

- first, second, and third functional units each having two inputs and an output; wherein

- the inputs of the first functional unit being coupled with the first and second register, respectively and the output with the fourth register;

- the inputs of the second functional unit being coupled with the second and third register, respectively and the output with the fifth register;

- the inputs of the third functional unit being coupled with the first and third register, respectively and the output with the sixth register; and wherein

the control unit performs a counter function on the first, second, and third registers such that the content of only one of the counter registers changes for each change in a counting sequence.

8. Counter arrangement according to claim 1, wherein the functional units perform a logical function.

9. Counter arrangement according to claim 1, wherein the functional units perform an arithmetic function.

10. Counter arrangement according to claim 7, wherein the functional units are EXCLUSIVE OR gates.

11. Counter arrangement according to claim 7, further comprising:

- an incrementer/decrementer unit having a control input for selecting an increment or a decrement function;

- a first select switch for coupling the incrementer/decrementer unit with one of the first, second, or third registers;

- an EXCLUSIVE OR gate having two inputs and an output, whereby the first input is coupled with the least significant bit of the first register and the second input is coupled with the least significant bit of the second register;

- a second select switch functionally coupled with the first select switch for coupling the output of the EXCLUSIVE OR gate, the least significant bit of the first register or a logical 0 with the control input of the incrementer/decrementer unit.

12. Counter arrangement according to claim 7, further comprising:

- a seventh, eighth, and ninth register;

- a first and second controllable inverter unit for either inverting or non-inverting a signal; and

- an EXCLUSIVE OR gate having two inputs and an output; whereby

- the first register is coupled with the seventh register;

- the second register is coupled through the first inverter unit with the eighth register;

- the third register is coupled through the second inverter unit with the ninth register; and whereby

- the least significant bit of the first register is coupled with the first input of the EXCLUSIVE OR gate and with the control input of the first inverter unit; and

- the least significant bit of the second register is coupled with the second input of the EXCLUSIVE OR gate whose output is coupled with the control input of the second inverter unit.

13. Counter arrangement according to claim 12, further comprising:

- a third and fourth controllable inverter unit; wherein

- the seventh register is coupled with the first register;

- the eighth register is coupled through the third inverter unit with the second register;

- the ninth register is coupled through the fourth inverter unit with the third register; and whereby

- the least significant bit of the seventh register is coupled with the control input of the third inverter unit; and

- the least significant bit of the eighth register is coupled with the control input of the fourth inverter unit.

14. Counter arrangement according to claim 13, wherein the seventh, eighth and ninth registers are concatenated and further comprising an incrementer/decrementer unit coupled with the concatenated registers.

15. Method for operating a counter comprising a plurality of counter registers and at least the same number of checksum registers, comprising the steps of:

- changing the value of only one of the counter registers with every change in a counting sequence;

- calculating the value of the associated checksum registers as a function of the content of at least two counter registers such that a checksum calculated from all checksum registers results in a constant value.

16. Method according to claim 15, wherein a logical function is used.

17. Method according to claim 15, wherein an arithmetic function is used.

18. Method according to claim 16, wherein an EXCLUSIVE OR function is used.

19. Method according to claim 15, wherein the step of changing the value further comprises the steps of:

- converting the content of all counter registers into binary code;
- incrementing or decrementing said binary code;
- converting said changed binary code back.

20. Method according to claim 19, wherein the step of converting the content into binary code comprises the steps of:

(a) selecting a most significant register;

(b) testing whether the content of the selected register is odd and if yes, inverting the content of the following register;

(c) ending the conversion if the following register is the least significant register;

(d) otherwise selecting the following register and repeating steps (b) through (d).

21. Method according to claim 19, wherein the step of converting the content from binary code comprises the steps of:

(a) selecting the register preceding the least significant register;

(b) testing whether the content of the selected register is odd and if yes, inverting the content of the following register;

(c) selecting the preceding register and repeating steps (b) through (c).

22. Method according to claim 15, wherein changing the value of one counter registers comprises the step of incrementing the value of the register by "1".

23. Method according to claim 15, wherein changing the value of one counter registers comprises the step of decrementing the value of the register by "1".

24. Method according to claim 15, wherein changing the value of one counter registers comprises the step of using a gray code for increments or decrements.

25. Method according to claim 15, wherein changing the value of the counter registers comprises the step of:

(a) incrementing a first register to its maximum value for each value change;

(b) incrementing a second register for the next value change; (c) decrementing the first register to its minimum value for each following value change;

(d) incrementing the second register for the next value change;

(e) repeating steps (a) through (d).

26. Method according to claim 15, wherein changing the value of the counter registers comprises the step of:

(a) decrementing a first register to its maximum value for each value change;

(b) decrementing a second register for the next value change;

(c) incrementing the first register to its minimum value for each following value change;

(d) decrementing the second register for the next value change;

(e) repeating steps (a) through (d).